

MIL-STD-1553 Remote Terminal DDC* enhanced mini-ACE* compatible core for FPGA Devices

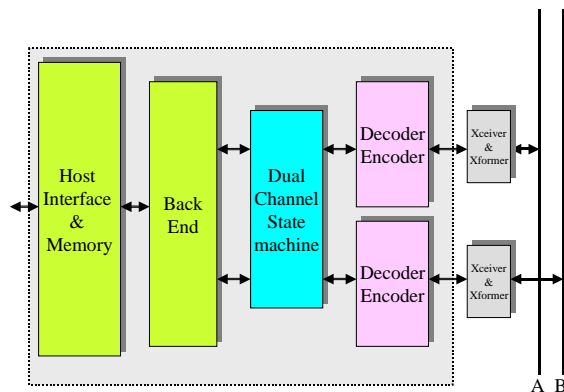
Feature Summary

- MIL-STD-1553B Notice 2 Remote Terminal (RT).
- Compatible with Industry standard **Enhanced DDC Mini-ACE*** host interface mapping and functionality.
- Best gate count in the industry.
- Supports any whole number clock frequency.
- Connects to any transceiver-transformer pair.
- Full MIL-STD-1553 Validation test passed in 3rd party tester.
- Vendor and technology independent IEEE-1076 VHDL design and coding.

An unflagging commitment to quality and excellence along with strict adherence to meeting the stringent requirements of the military specifications have been the guidelines for Sital Technology's MIL-STD-1553B notice 2 RT core.

Sital Technology's *1553 RT core* is a uniquely portable and flexible solution, based on an innovative vendor independent architecture, for any EPLD/FPGA device.

RT Block Diagram



Host Interface

The remote terminal host interface memory and register map is compatible with *DDC's enhanced mini ACE** Remote Terminal mapping. For reasons of FPGA space optimization, not all of DDC's features were implemented. The 4 communication modes of operation, single buffer, dual buffer, circular buffer and global circular buffer modes are controllable

on a sub-address by sub-address manner compatible with DDC's memory mapping. FPGAs, being a flexible technology allows Sital to add additional compatibility features if such are required.

Manchester Decoder

The unique Manchester decoder can work with any whole number clock frequency from 12Mhz and up. (For example it could work with a PCI interface's 66 Mhz clock)

Gate Count

Vendor*	Product Family*	Used Logic
Altera	Cyclone	1,510 LEs
Altera	Stratix	1,506 LEs
Xilinx	Spartan2E	893 Slices
Xilinx	Virtex II	890 Slices

Transceivers

Sital Technology's *1553 RT core* connects to any standard transceiver-transformer pair. The core was fully validated with a 3rd party dual transceiver.

RT Validation

Sital Technology's *1553 RT core* has been successfully implemented in a 3rd party FPGA, and has passed the full MIL-STD-1553B Notice 2 RT Validation test plan in an independent laboratory.

Licensing

Sital Technology's *1553 RT core* uses a unique method to ease the licensing of the core. We have eliminated the cost of ownership, meaning there is no initial payment for the core. A pay per use business model is implemented, making it very simple, straightforward and cost effective.

For more information please visit our Web page www.sital.co.il/1553.html

*Products and company names listed are trademarks or trade names of their respective companies.