



SITAL Technical Notes

Simulating Altera Quartus VHDL Gate-Level file in Modelsim

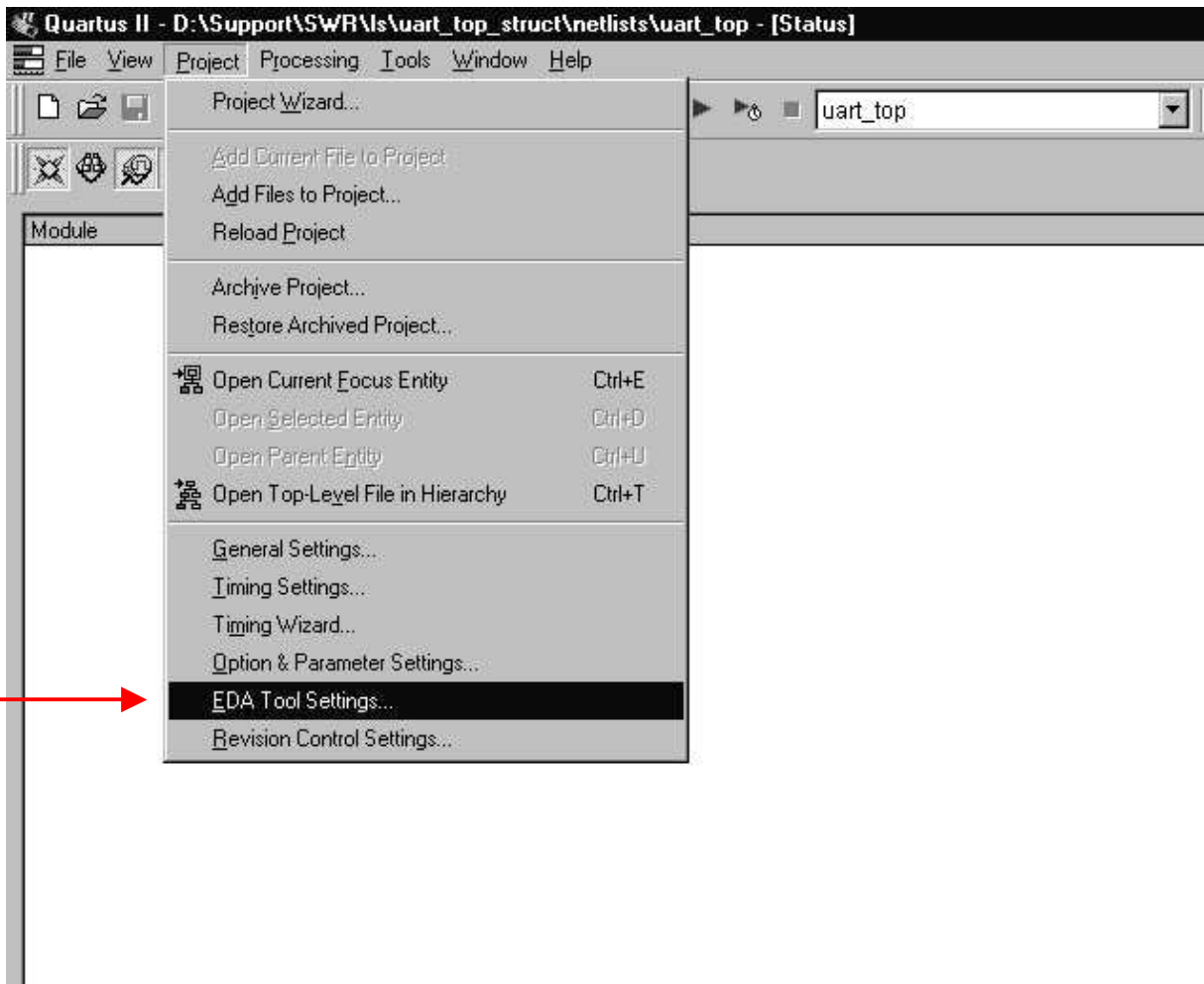


NOTE: This document is relevant for Quartus II version 1.1 and further versions. For other version please contact ‘SITAL Technology’.

In order to simulate a VHDL gate-level file that was generated by the Altera Quartus II tool, please do the following steps:

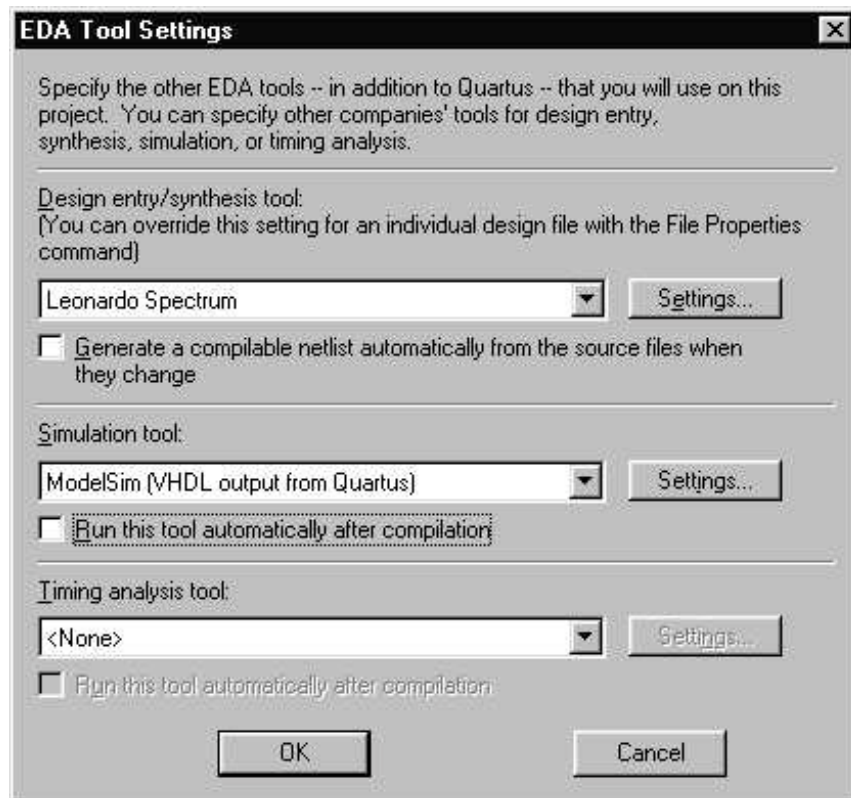
1. Produce the VHDL Output file (.vho) & the Standard Delay Format Output file (.sdo) from the Altera Quartus II .

- a) In the Quartus tool, please create a new project or open an existing project from the file menu
- b) Choose **EDA Tool Setting** from the **Project** menu .





- c) In the Simulation tool list ,select ‘**Modelsim (VHDL output from Quartus)**’.



- d) Press **OK** .
e) Continue and run your Place & Route process.
f) At the end of the P&R process you will get 2 files: ***.vho** , ***.sdo** .

These files contains the Vhdl description and the timing information of your desgin.

2. Generate the Altera primitives library.

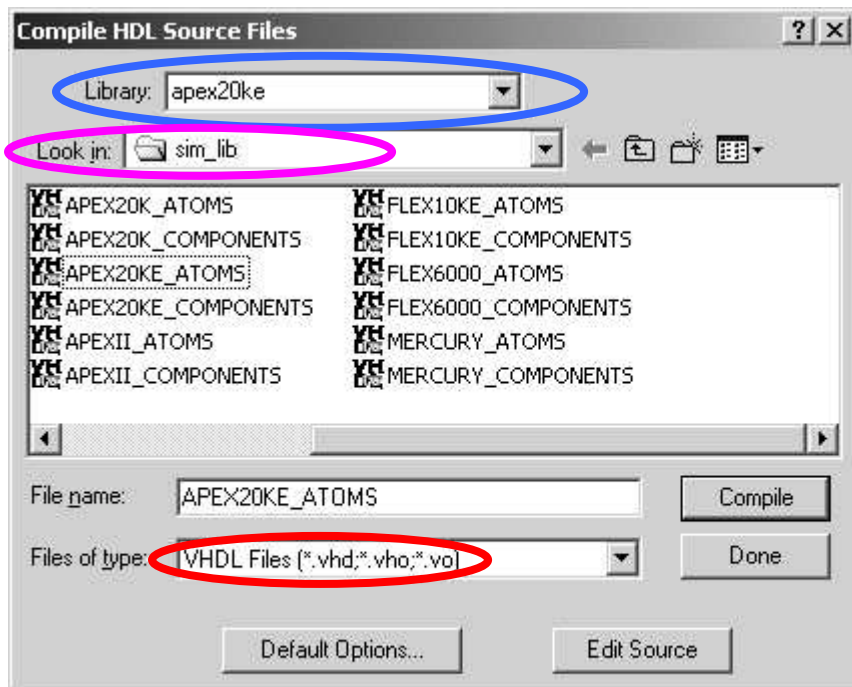
The VHDL gate-level file (*.vho) is using the Altera primitives library.

Please do the following steps to generate this library:

- a) Invoke the ModelSIM Simulation tool.
- b) Within the Transcript text window do the following:
- c) Change Directory to the ModelSIM Installation dir, for example C:/modeltech_5.5e.
cd C:/Modeltech_5.5e
- d) Using windows explorer, change the modelsim.ini file properties (located at **C:/Modeltech_5.5e**) for write permission.
- e) According to your <device family>, generate a new library using the Vlib command.
For example if your <device family> is **apex20ke** then use the command :
vlib apex20ke



- f) Map the new library using the Vmap command:
vmap <device family> C:/Modeltech_5.5e/ <device family>
if your ModelSIM Installation directory is different than c:/modeltech_5.5e,
then type:
vmap <device family> your_modelsim_installation_directory/<device family>
- g) In **C:/Modeltech_5.5e** change back modelsim.ini properties for read only.
- h) Change Modelsim directory to: **../quartus/eda/sim_lib**.
- i) Compile the Altera primitives source files:
Select the **'Design > Compile'** button,
In the **'Compile HDL Source Files'** dialog box set the library to your
<device family>library name, using the pull down menu.
Use the **'Look in'** selection to locate the **'VHDL ATOMS'** source files.



Compile the sources according to your <device family>.
For example if your <device family> is **APEX20KE**,
first compile the **APEX20KE_ATOMS.VHD** file,
then compile the **APEX20KE_COMPONENTS.VHD** file.

- j) The Altera primitives library of your <device family> is ready.



3. Gate-level simulation without timing information.

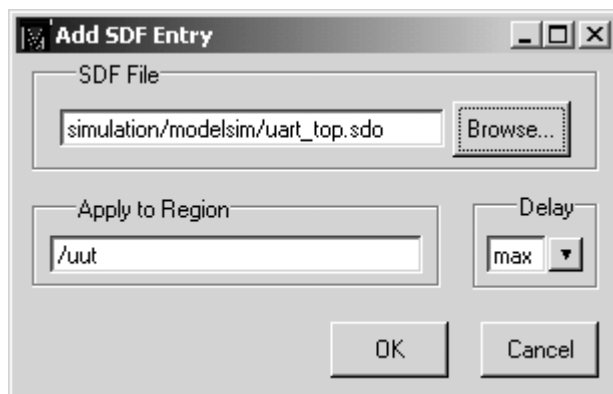
To Simulate your gate-level file **without** timing information do the following:

- Copy the *.vho file into your project directory.
- Change ModelSIM directory to your project directory.
- Compile the VHDL gate-level file (*.vho) into your work library, using the vcom command (**vcom *.vho**) or from the Compile window.
- Simulate your Test-Bench.

4. Gate-level simulation with timing information.

To Simulate your gate-level file **with** timing information do the following:

- Steps 2.a - 2.c as described above.
- In Modelsim main toolbar select '**Design > Load Design**'.
- In the '**SDF**' folder select the '**Add**' option. Specify the full path to the sdf file
→ *.sdo .



- Insert the **Instance** name of your Entity in the '**Apply to region**' field. The instance name is the name you have gave to your component during the Port Map command in your Test Bench. For example:

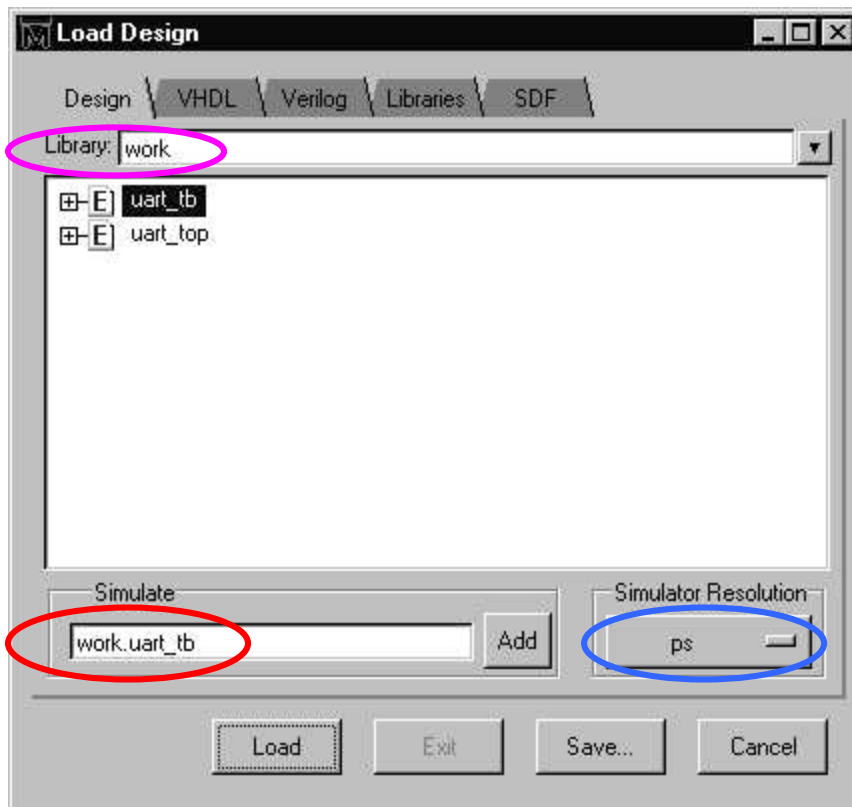
UUT: uart_top
Port map (.....

UUT is the instance name, so you have to apply the SDF file to this region by assigning '/UUT' in the 'Apply to region' field.

- Select **OK**.



- g) In the '**Design**' folder, Change the '**Simulator Resolution**' to '**ps**'.
- h) Set the library field to **work** and select your Test-Bench entity, click the '**Add**' button.



- i) Select the '**Load**' button to perform a gate-level timing simulation.

You may also load your design using a text command instead of using the GUI as described in sections 3 by typing the following:

```
vsim -t ps -sdfmax UUT=D:/VHDL_Work/Uart/uart_top.sdo work.uart_tb
```