



SITAL Technical Notes

Simulating Altera Max-Plus II VHDL Gate-Level file in Modelsim



In order to simulate a VHDL gate-level file that was generated by the Altera MaxPlus II tool, please do the following steps:

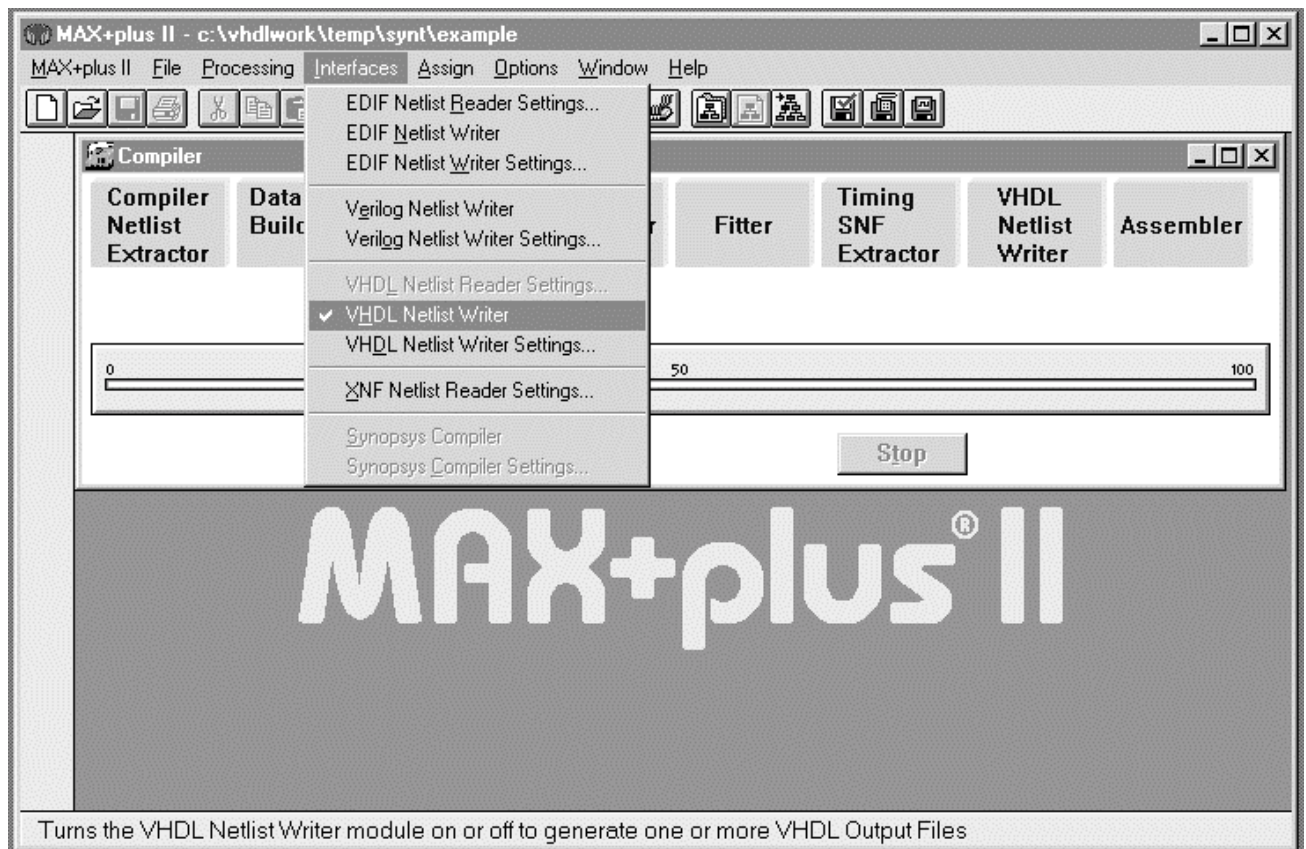
The Altera MAXplus II tool suggest two methods for gate-level VHDL simulation:

- VHDL file with the timing information in it.
- VHDL file and a separate SDF timing file.

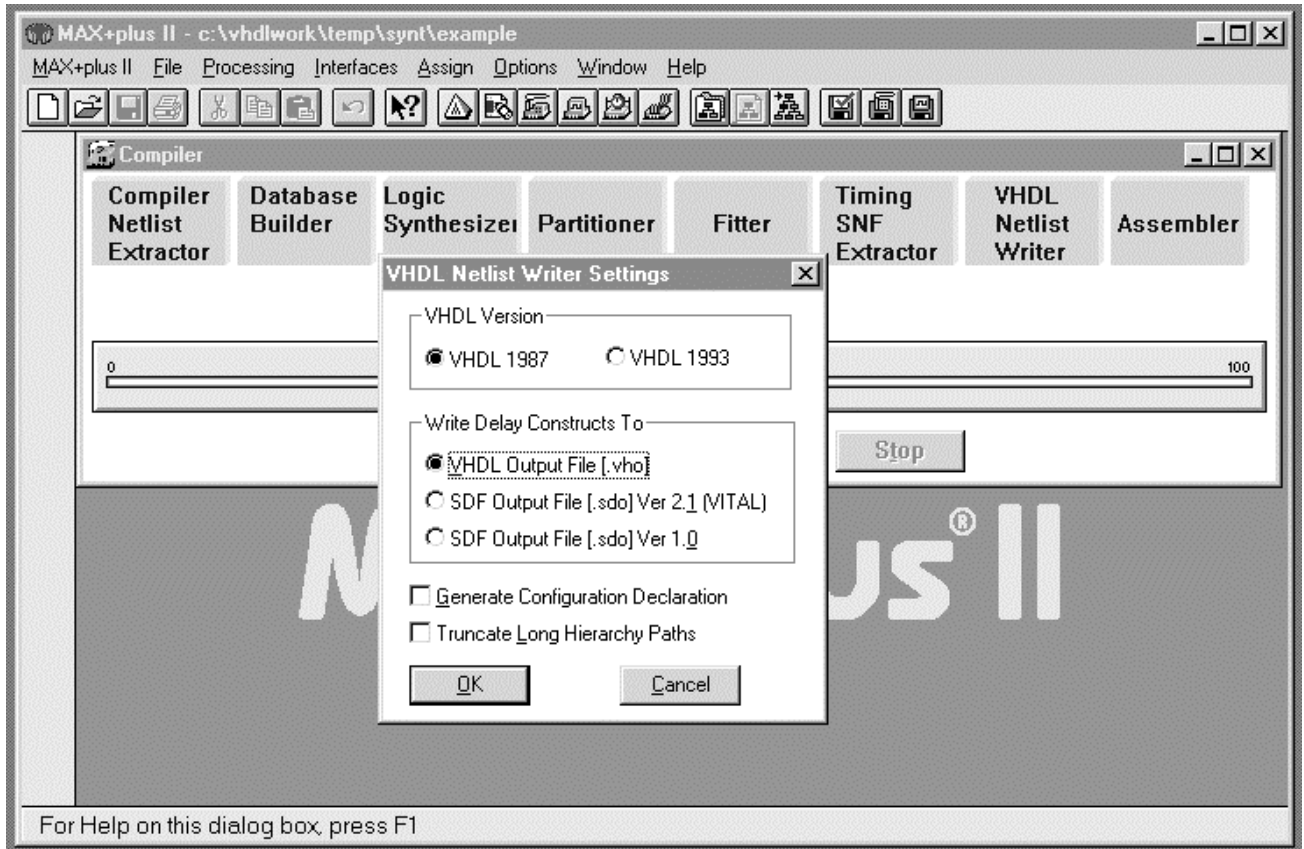
This application note will describe how to generate and simulate a gate-level file that contain the timing information in it.

1. Produce the VHDL gate-level file with the delay information in it in the MAXplus II tool.

- a) Set the 'VHDL Netlist Writer' option in the MAXplus II Compiler Interfaces menu:



- b) Assign to MAXplus to Write Delay Constructs To 'VHDL Output File [.vho]'. This form will appear when the 'VHDL Netlist Writer Settings' option is selected from the MAXplus II Compiler Interfaces menu.



At the end of the MAXplus II process you will receive 1 VHDL file named:
Your_entity_name.vho

This file contains the VHDL description and the timing information of your design.

2. Gate-level simulation with timing information.

To simulate your gate-level file with timing information do the following:

- a) Within the Transcript window of ModelSIM, change directory to your source environment.
- b) Compile the VHDL gate-level file (your_entity_name.vho) into your work library.
vcom your_entity_name.vho
- c) Simulate your Test-Bench.