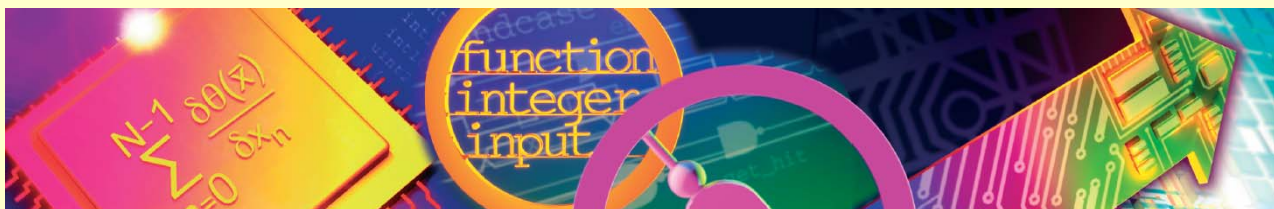


# Welcome to Israel Solutions Expo 2007



Join Mentor Graphics at the

Solutions Expo 2007 Conference on Sunday December 2<sup>nd</sup>, at the Hilton Tel-Aviv Hotel.

The Solutions Expo is a great chance to discover the latest EDA technology news and design solutions. During the day you will have the opportunity to meet senior Mentor Graphics management and experts from our technical teams. Aimed at engineers and managers, the conference is open to both customers and the design community at large, allowing you to share design and system integration experiences with engineers from a wide variety of companies.

## No conference fee

Attendance at this annual event is free (Lunch is included), but you will need to register in advance.

## General Session

The Keynote Speaker will be:

**Mr. Walden C. Rhines - CEO & Chairman of the Board, Mentor Graphics.**

## Technical Session

We are going to have technical sessions from 10:20 till 16:20 covering : Design to Silicon Platform, IC Nanometer, Functional Verification, ESL to Prototyping, PCB System Design and Embedded Software Design.

Some of the technical sessions will be presented by Mentor product managers:

**Mr. Henry Potts, Vice President & General Manager - System Design Division.**

Mr. Simon bloch, General Manager - Design Creation and Synthesis Division.

## Mentor Partners

Sital Technology - Our distribution partner for HDL & PADS design tools.

Altera & Xilinx

**We look forward to meeting you at this year's Solutions Expo!**

**Elisha Wertman**  
**Country Manager,**  
**Mentor Graphics Israel.**

# Mentor Graphics Solutions Expo/Seminar 2007 - Israel

Sunday December 2<sup>nd</sup> ,2007

Hilton Hotel – Tel Aviv



## AGENDA

8:20 – 9:00	<b>Registration</b>						
9:00 – 9:15	<b>Welcome Note</b>						
9:15 – 9:50	<b>Design for the Nanometer Age: New Challenges, New Opportunities</b> - Walden C. Rhines, CHAIRMAN & CEO , Mentor Graphics						
9:50 – 10:20	<b>Coffee Break</b>						
	<b>PCB System Design</b>	<b>Functional Verification</b>		<b>ESL to Prototyping</b>	<b>Nanometer IC Design</b>	<b>Design to Silicon Platform</b>	<b>Embedded Software Design</b>
10:20 – 11:10	Innovation - The challenge of the PCB design industry  Henry Potts, VP& GM System Design Division	Achieving Optimal Designs though Electronic System Level (ESL) Methodologies  Simon Bloch, GM Design Creation and Synthesis Division			Variability driven netlist-to-GDS2 design closure platform ; 65/45nm routing and manufacturing closure	Calibre LVS and Calibre xRC: Comprehensive Parameter Extraction: Device and Interconnect Modeling	Nucleus Suite for FPGA & SoC
11:10 – 12:00	PCB Flow - 2007 Update	Functional Verification: The Road Ahead  John Lenyo, Director of Marketing - Design Verification Division		Reducing Test Cost and Power aware techniques in Manufacturing Test	Leveraging Fast-SPICE Technology for Full-chip Mixed-signal SoC Verification	Calibre DRC: Redefining the Meaning of Sign-off	EDGE Developer Suite
12:00 – 13.30	<b>Lunch</b>						
13:30 – 14:20	High-Speed Update: New Solutions for Signal Integrity, Timing, Power Integrity	Managing Verification through Coverage-Driven Closure		Achieving Increased Productivity with New Synthesis Techniques for FPGA & ASIC Prototyping	Partnering Design and Test to Reach Zero Defective Parts per Million (DPM)	Calibre LFD: Litho-Hotspot Simulator for Designers: A Reality Starting at 65nm!	Inflexion Platform UI
14:20 – 15:10	Design and Library Management using DMS	Finding and Eliminating Real Functional Problems with 0-in CDC Verification		Catapult C Synthesis: A Proven Methodology for Complex Hardware Creation	Accelerating Customer IC Layout: Speed without Compromise	The Power of Customer Validation: Calibre DFM Tools and Methodologies	RTOS: Concept & Evolution
15:10 – 15:30	<b>Coffee Break</b>						
15:30 – 16:20	Integrated RF Design	Functional Verification of Low Power Designs	Formal: Improve your Functional Verification Quality	CodeLink: Fast Execution and Source-Level Debug of Embedded Processor or DSP	Efficient Full-chip Mixed-signal Verification by Leveraging Fast-SPICE Technology	Electrical DFM: Next Generation Parametric Yield Prediction	

# Welcome to Israel Solutions Expo 2007

To register to attend the **Israel Solutions Expo 2007** on **December 2<sup>nd</sup>**, please supply your contact details and indicate which presentations you would like to attend and send the registration form to us as soon as possible, November **27<sup>th</sup>** at the latest.

## Send the REGISTRATION

By WEB : [www.mentor.com/events/solexpo/israel](http://www.mentor.com/events/solexpo/israel)

By e-mail to : [info\\_isr@mentor.com](mailto:info_isr@mentor.com)

By fax to : 09-9552627 . Please make a copy of this page.

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I will be attending and would like to register for the following breakouts:

### 10:20 - 11:10

<input type="checkbox"/> <b>PCB-1</b> Innovation	<input type="checkbox"/> <b>FV-1</b> ESL Method's	<input type="checkbox"/> <b>ESL-1</b> ESL Method's	<input type="checkbox"/> <b>Nano-1</b> Sierra	<input type="checkbox"/> <b>D2S -1</b> Calibre LVS	<input type="checkbox"/> <b>ESD-1</b> Nucleus
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### 11:10 - 12:00

<input type="checkbox"/> <b>PCB-2</b> 2007 update	<input type="checkbox"/> <b>FV-2</b> Func Verf	<input type="checkbox"/> <b>ESL-2</b> Func Verf	<input type="checkbox"/> <b>Nano -2</b> TK – Xpress	<input type="checkbox"/> <b>D2S -2</b> Calibre DRC	<input type="checkbox"/> <b>ESD-2</b> Edge
			<input type="checkbox"/> <b>Nano -2</b> Fast-Spice		

### 13:30 - 14:20

<input type="checkbox"/> <b>PCB-3</b> High Speed	<input type="checkbox"/> <b>FV-3</b> Coverage	<input type="checkbox"/> <b>ESL-3</b> Synthesis	<input type="checkbox"/> <b>Nano -3</b> Zero DPM	<input type="checkbox"/> <b>D2S -3</b> Calibre LFD	<input type="checkbox"/> <b>ESD-3</b> Inflexion UI
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### 14:20 - 15:10

<input type="checkbox"/> <b>PCB-4</b> Library Mgmt	<input type="checkbox"/> <b>FV-4</b> 0-In CDC	<input type="checkbox"/> <b>ESL-4</b> Catapult C	<input type="checkbox"/> <b>Nano -4</b> IC Layout	<input type="checkbox"/> <b>D2S -4</b> Calibre DFM	<input type="checkbox"/> <b>ESD-4</b> RTOS
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### 15:30 - 16:20

<input type="checkbox"/> <b>PCB-5</b> RF Design	<input type="checkbox"/> <b>FV-5</b> Low Power	<input type="checkbox"/> <b>ESL-5</b> CodeLink	<input type="checkbox"/> <b>Nano -5</b> Mix-Signal	<input type="checkbox"/> <b>D2S-5</b> Electrical DFM	
	<input type="checkbox"/> <b>FV-5</b> Formal				

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Name \_\_\_\_\_

Title \_\_\_\_\_

Company \_\_\_\_\_

Phone \_\_\_\_\_ Fax \_\_\_\_\_

E-mail \_\_\_\_\_