

Welcome to Israel Solutions Expo 2008



Join Mentor Graphics at the

Solutions Expo 2008 Conference on Tuesday November 18th, at the Hilton Tel-Aviv Hotel.

The Solutions Expo is a great chance to discover the latest EDA technology news and design solutions. During the day you will have the opportunity to meet senior Mentor Graphics management and experts from our technical teams. Aimed at engineers and managers, the conference is open to both customers and the design community at large, allowing you to share design and system integration experiences with engineers from a wide variety of companies.

No conference fee

Attendance at this annual event is free (Lunch is included), but you will need to register in advance.

General Session

The Keynote Speaker will be:

Mr. Hanns Windele - Vice President Europe, Mentor Graphics

Technical Session

You will be able to attend technical sessions from 10:20 till 16:20 covering : IC Design & Verification, Functional Verification, ESL to Prototyping, SOC Design & Verification ,PCB System Design and Embedded Software Design.

The first technical session for PCB will be presented by:

Mr. Henry Potts, Vice President & General Manager - System Design Division.

Mentor Partners

Sital Technology - Our distribution partner

Altera

MunEDA

Synterix Technology



Registration is at www.mentor.com/events/solexpo/israel/

If you need to register by fax, pls contact us by email info_isr@mentor.com or call 09-9718642/3

We look forward to meeting you at this year's Solutions Expo!

Elisha Wertman
Country Manager,
Mentor Graphics Israel.



Mentor Graphics Solutions Expo/Seminar 2008 - Israel

Tuesday November 18th, 2008

Hilton Hotel – Tel Aviv



AGENDA

8:20 – 9:00	Registration					
9:00 – 9:15	Welcoming introduction					
9:15 – 9:50	A demographic driven design evolution - Hanns Windele, Vice President Europe , Mentor Graphics					
9:50 – 10:20	Coffee Break					
	PCB System Design	Functional Verification	ESL to Prototyping	IC Design & Verification - A	IC Design & Verification - B	Embedded Software Design
10:20 – 11:10	Collaborate or Risk Extinction Henry Potts, VP& GM System Design Division	Advancing Verification Productivity & Debug with Questa	Innovative ESL HW/SW Design Flow for Low-Power SoCs	Reducing Cycle Time in Physical Verification	Olympus-SoC Overview: The Power of Multi-Corner/Multi-Mode P&R for Timing, Power, SI & MFG Closure (part 1)	Nucleus RTOS - Makes Good Design Sense
11:10 – 12:00	BGA Breakouts and Routing (part 1)	Closing the Verif Loop with InFact Intelligent Testbench Automation & Questa Multi-View Components	Catapult C Synthesis: ESL Methodology & Low Power Design	Model Based DFM: 2D/3D Variability Analysis/Optimization	Olympus-SoC Overview: The Power of Multi-Corner/Multi-Mode P&R for Timing, Power, SI & MFG Closure (part 2)	Nucleus USB Stack - Meet all of your design challenges with extensive USB connectivity & support
12:00 – 13:30	Lunch					
13:30 – 14:20	BGA Breakouts and Routing (part 2)	Functional Verification and Debug of MIPS and ARM Based Multi-Core SoC	Innovation in FPGA Synthesis	IC yield improvement: How designers can solve MFG issues at 65nm, 45nm and below	Advanced Manufacturing Test Solutions	
14:20 – 15:10	PCB Power Delivery optimization and DDR3 verification with HyperLynx 8.0	Simplifying Testbench Creation with Certe for Advanced Verification Methodologies: OVM, AVM, SV.	Accelerating Design Reuse with HDL Designer: Code Quality Metrics, IP-XACT, Auto-Doc, and More	Advanced ERC/ESD checks using Calibre PERC	Power Aware ATPG and Low Pin Count Testing	
15:10 – 15:30	Coffee Break					
15:30 – 16:20	Multi-Discipline Collaboration - Teamwork beyond PCB	Finding the Toughest Bugs with 0-in@ CDC and Formal Verification	Tracing Requirements from System Level to Subsystem Implementation & Verification with ReqTracer	Manufacturing Variability and its Impact on Timing, Power		
16:20 – 16:30	Closing and Prize Draw					