

# SystemVerilog for Verification & Design

## Course Overview

SystemVerilog is the most transformative technology in EDA since the birth of logic synthesis. It is an extension of the popular Verilog language, bringing a higher level of abstraction to design and verification. SystemVerilog provides a complete verification environment, employing Constraint Random Generation, Assertion Based Verification and Coverage Driven Verification. These methods improve dramatically the verification process. SystemVerilog also provides enhanced hardware-modeling features, which improve the RTL design productivity and simplify the design process.

This comprehensive training will explore the SystemVerilog language and demonstrate how to build a complete verification environment using Random generation, Assertion Based Verification and Functional Coverage. Students will learn how to take advantage of the SystemVerilog language to improve their RTL design and become more productive. Tutorials and workshops focusing on the language features are combined in the course. Graduates will be able to use any simulation or synthesis tool that support SystemVerilog.

For more information about SystemVerilog, please visit: [www.sital.co.il/systemverilog](http://www.sital.co.il/systemverilog)

## Participants

The course is targeted to hardware (VHDL and Verilog) designers and verification engineers who wish to start using SystemVerilog.

## Prerequisites

Participants must be familiar with the Verilog Language. Experienced VHDL designers or verification engineers with no Verilog knowledge may achieve the required basic Verilog knowledge by self-studying the Verilog primer module at: <http://www.sital.co.il/basicveriloglearning>

This course is not suitable as a beginner's course. Students requiring a thorough understanding of Verilog or VHDL should attend the Basic Verilog or VHDL training.

## Course Material

- The course slides book.

## Course Tutors

SITAL Technology trainers - experts in Verilog and VHDL design and Verification, will lecture the course.



## Course Details

### Introduction

- History of Verilog HDL
- What is SystemVerilog
- Verification Methodology
- SystemVerilog Verification Environment

### Language overview

- 2001 structures
- Data types
- Array
- Struct/union
- Module and interface
- Operators
- Event scheduling in Verilog 2001
- Event scheduling in System Verilog
- Program

### Data generation

- Direct data generation
- Simple random generation
- Class and class inheritance
- Random variables
- Random options
- Constrained random
- Weighted randomization
- Random sequence

### Driver

- Driver concept
- Tasks and functions in BFM
- Clocking block
- Bind program to a module

### Functional Coverage

- What is Functional Coverage
- How to apply Functional Coverage
- Data and Control oriented coverage
- Covergroup
- Coverpoint and bins
- Covergroup methods, options and system tasks

### Checker

- Checker concept
- Collector
- Scoreboard
- Constraint as checkers
- Queue
- Associative array

### SystemVerilog Assertions

- Assertion based verification
- Immediate assertions
- Concurrent assertions
- The ##, |->, |=> operators
- Property
- Sequence
- Operations
- Assertion directives

### Appendix

- Code reuse
- Interface to VHDL
- DPI

- A workshop is combined in each of the 3 days course, exercising students in taking a design through the entire verification process from specification to the implementation of a coverage driven, constraint random, assertion based verification environment.
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