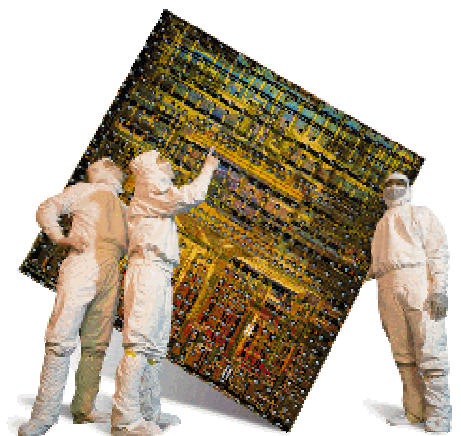




SITAL Technical Notes

Simulating Xilinx Timing VHDL Gate-Level file in Modelsim

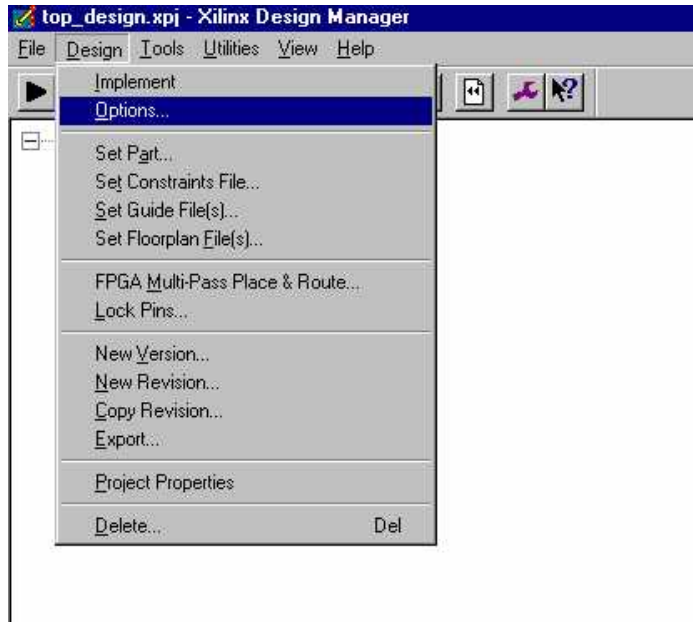




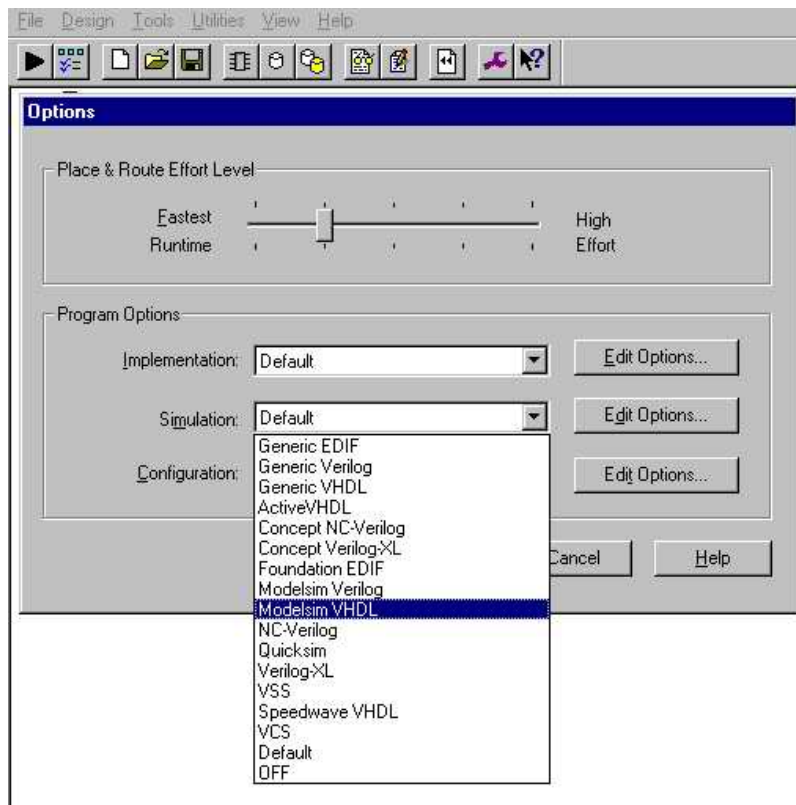
In order to simulate a VHDL gate-level VITAL file that was generated by the Xilinx Design Manager, please do the following steps:

1. Produce the VHDL gate-level VITAL file & the SDF delay file from the Xilinx Design Manager.

a) In the 'Design' menu select 'Options':

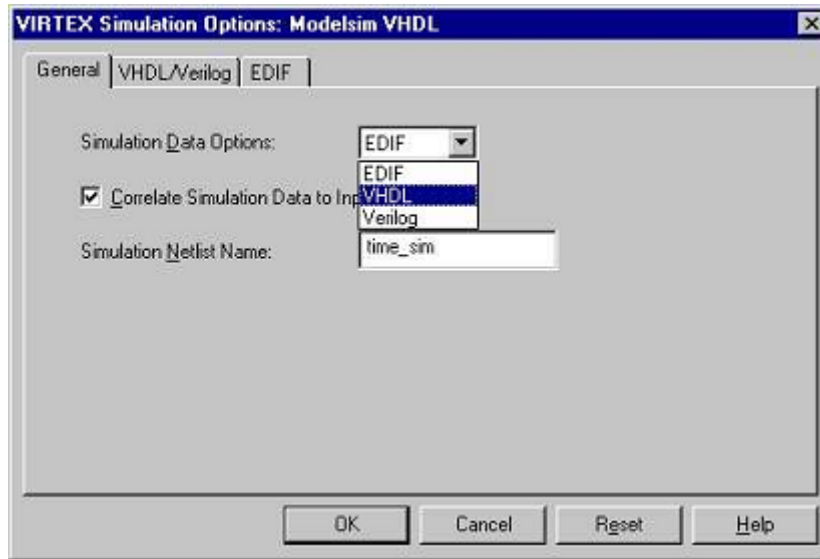


b) Set 'simulation' to 'Modelsim VHDL' and then press the 'Edit Options' :





c) Set 'Simulation Data Option' to 'VHDL':



d) Continue and run your Place & Route process.

e) At the end of the P&R process you will get 2 files:

Time_sim.vhd ,
Time_sim.sdf

These files contains the Vhdl description and the timing information of your desgin.



2. Generate the Xilinx SIMPRIM library.

The VHDL gate-level file (Time_sim.vhd) is using the Xilinx primitives library. Please do the following steps to generate the Xilinx SIMPRIM library:

- a) Invoke the ModelSIM Simulation tool.
- b) Within the Transcript text window do the following:
- c) Change Directory to the ModelSIM Installation dir, for example C:/modeltech_5.5e.
cd C:/Modeltech_5.5e
- d) In C:/Modeltech_5.5e change modelsim.ini properties for write permission.
- e) Generate a new library called SIMPRIM using the Vlib command:
vlib SIMPRIM
- f) Map the new library using the Vmap command:
vmap SIMPRIM C:/Modeltech_5.5e/SIMPRIM
if your ModelSIM Installation directory is different than c:/modeltech5.5c, then type:
vmap SIMPRIM your_modelsim_installation_directory/SIMPRIM
- g) In C:/Modeltech_5.5e change back modelsim.ini properties for read only.
- h) From Windows Explorer, Verify that the following files exist:
../xilinx/vhdl/src/simprims/**simprim_Vpackage_mti.vhd**
../xilinx/vhdl/src/simprims/**simprim_Vcomponents_mti.vhd**
../xilinx/vhdl/src/simprims/**simprim_VITAL_mti.vhd**
- i) Go back to the ModelSIM Transcript window.
- j) Change directory to: ../xilinx/vhdl/src/simprims.
- k) Type the following compile commands:
vcom -work SIMPRIM simprim_Vpackage_mti.vhd
vcom -work SIMPRIM simprim_Vcomponents_mti.vhd
vcom -work SIMPRIM simprim_VITAL_mti.vhd
- l) The SIMPRIM Library is ready.

2. Gate-level simulation without timing information.

To Simulate your gate-level file **without** timing information do the following:

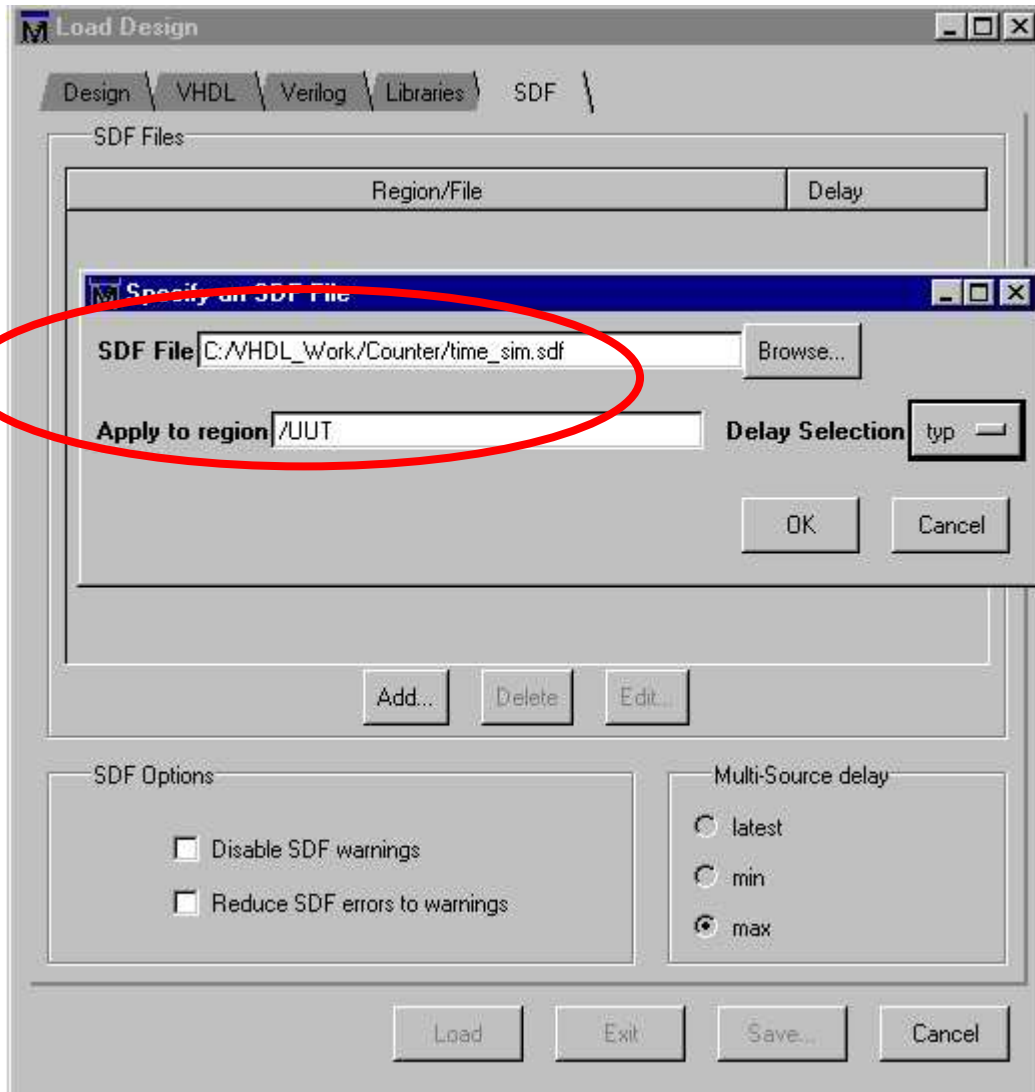
- a) Copy the **Time_sim.vhd** file into your project directory.
- b) Change ModelSIM directory to your project directory.
- c) Compile the VHDL gate-level file (Time_sim.vhd) into your work library, using the vcom command (**vcom time_sim.vhd**) or from the Compile window.
- d) Simulate your Test-Bench.



3. Gate-level simulation with timing information.

To Simulate your gate-level file **with** timing information do the following:

- e) Steps 2.a & 2.c as described above.
- b) In Modelsim main toolbar select '**Design > Load Design**'.
- c) In the '**SDF**' folder select the '**Add**' option. Specify the full path to the sdf file
→ Time_sim.sdf .



- d) Insert the **Instance** name of your Entity in the '**Apply to region**' field. The instance name is the name you have gave to your component during the Port Map command in your Test Bench. For example:

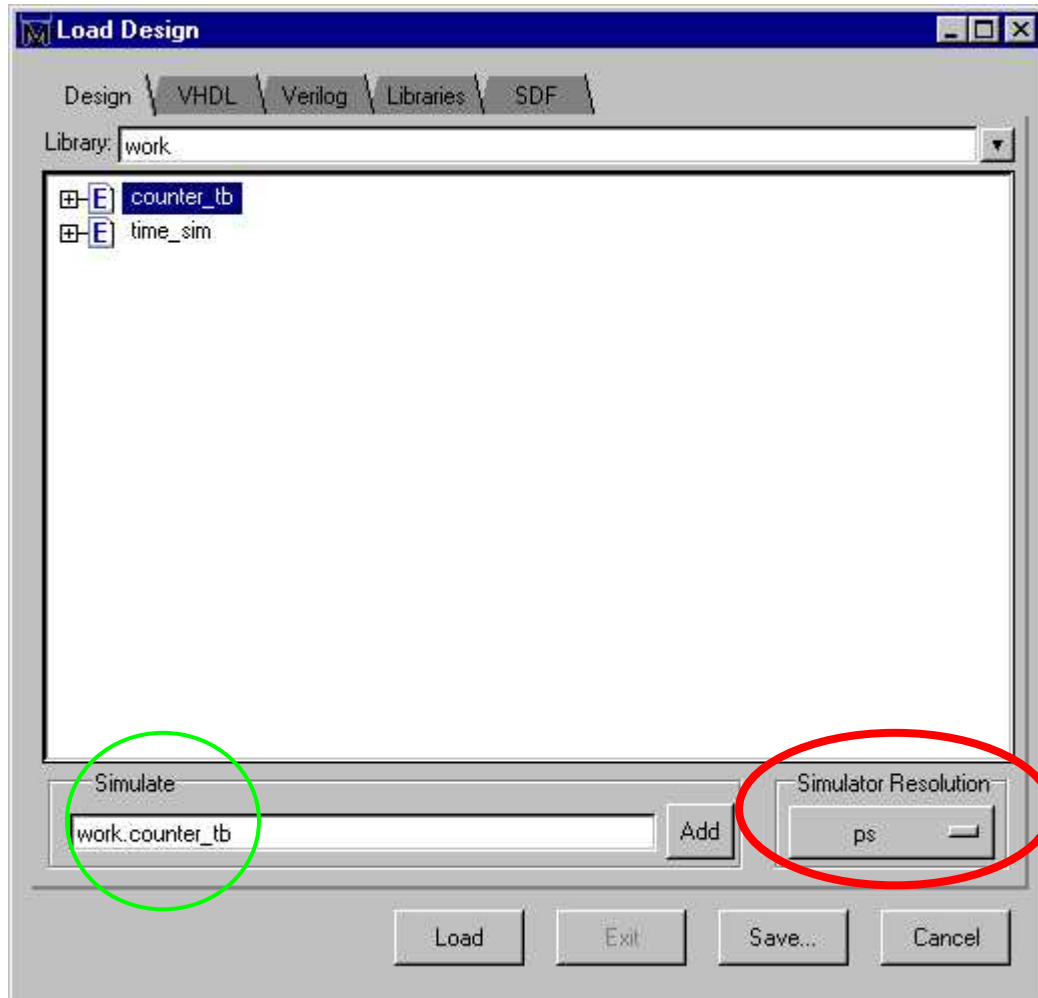
UUT: counter
Port map (.....

UUT is the instance name, so you have to apply the SDF file to this region by assigning '/UUT' in the 'Apply to region' field.

- f) Select **OK**.



- g) In the '**Design**' folder, Change the '**Simulator Resolution**' to '**ps**'.
- h) Set the library field to **work** and select your Test-Bench module, click the '**Add**' button.



- i) Select the '**Load**' button to perform a gate-level timing simulation.

You may also load your design using a text command instead of using the GUI as described in sections 3 by typing the following:

```
vsim -t ps -sdfmax UUT=D:/VHDL_Work/Counter/time_sim.sdf work.counter_tb
```