



SITAL Technical Notes

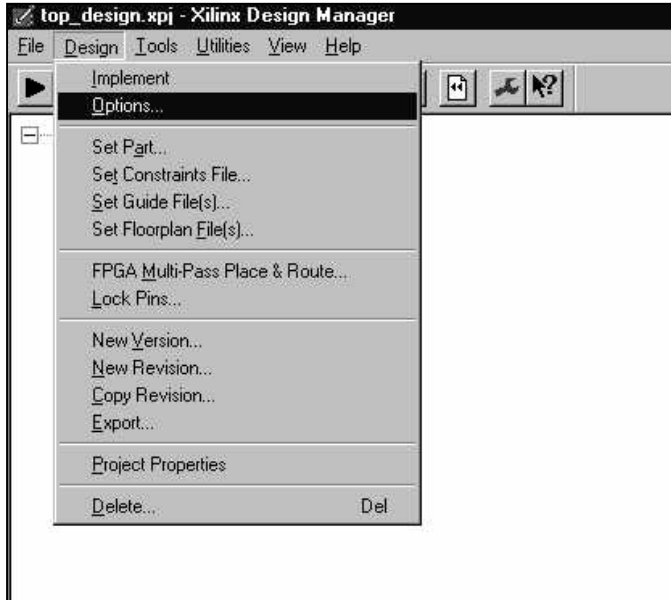
Simulating Xilinx Timing Verilog Gate-Level file in Modelsim



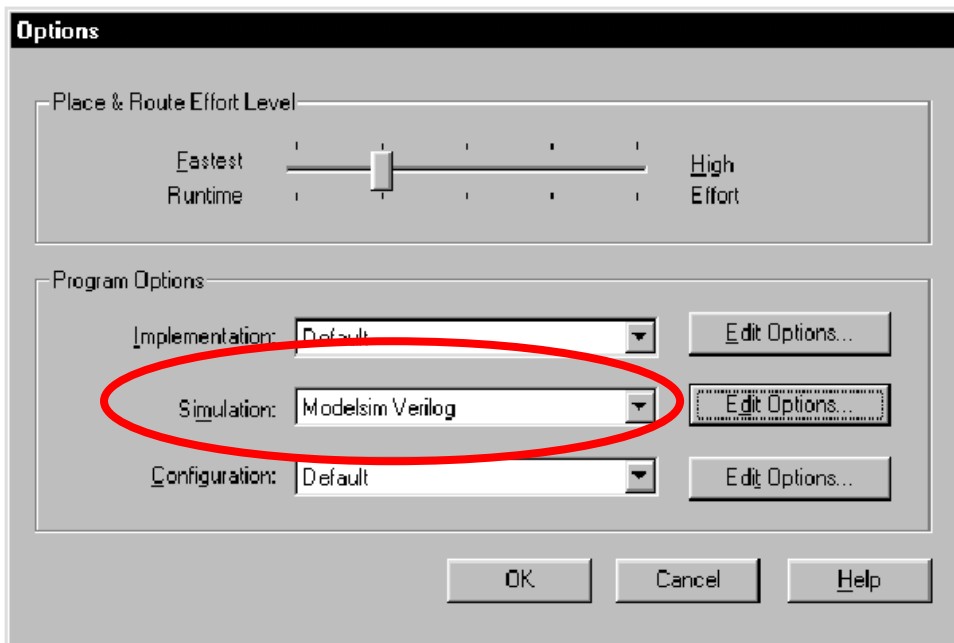
In order to simulate a Verilog gate-level file that was generated by the Xilinx Design Manager, please do the following steps:

1. Produce the Verilog gate-level file & the SDF delay file from the Xilinx Design Manager:

- a) From Xilinx Design Manager tool select **'Design > Options...'**



- b) Set the **Simulation** option to **'Modelsim Verilog'**:



- c) Continue and run your Place & Route process.



d) At the end of the P&R process you will get 2 files:

Time_sim.v , Time_sim.sdf

These files contains the Verilog description and the timing information of your desgin.

2. Generation of the Xilinx SIMPRIM library.

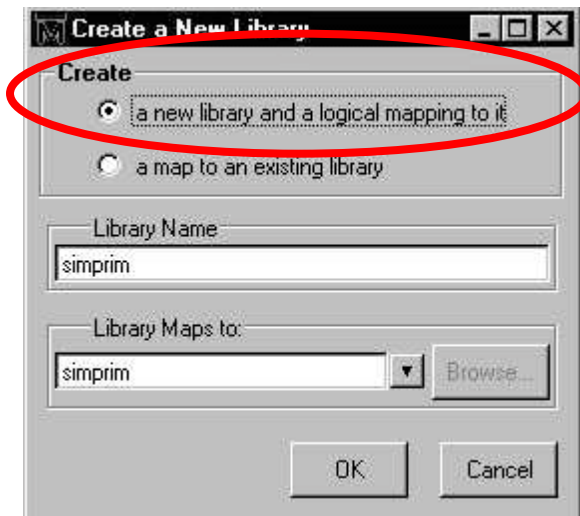
The SIMPRIM libraries are required for gate-level simulation.

The Verilog source code can be found at: **Xilinx_installation_dir/verilog/src/simprims.**

This directory contains the all the *.v model files for the simprim library.

These libraries are used for the timing simulation of any Xilinx device family.

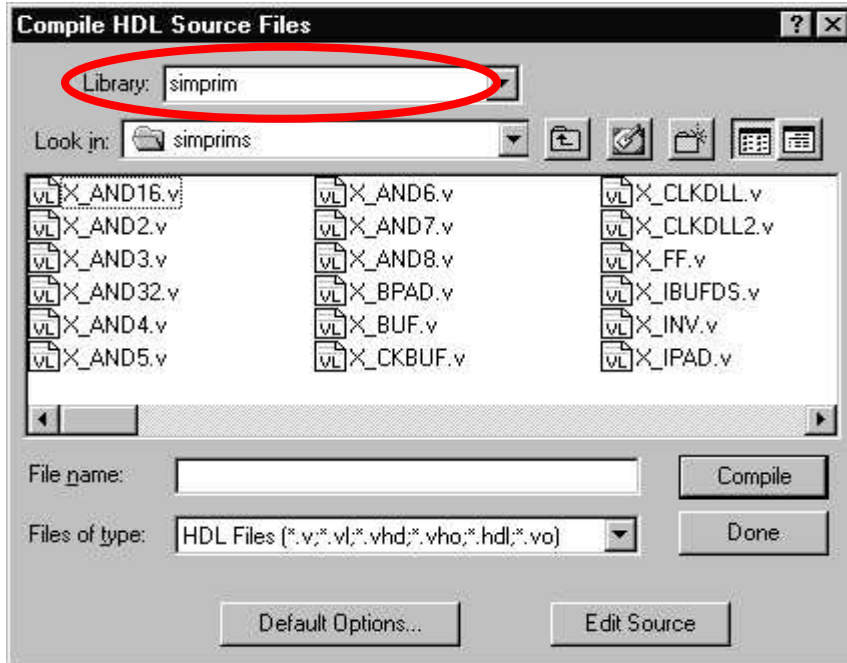
- a) Run the ModelSIM Simulation tool.
- b) Change into the directory in which you wish to store the SIMPRIM compiled libraries. Select **'File > Change Directory'**, use the file browser to locate a desired directory. Any library that is now created will be placed into this directory by default.
- c) Create the simprim library. Select **'Design > Create a New Library'**, ensure that **'a new library and logical mapping to it'** is selected. Enter 'simprim' in the library name box as shown below:



d) Select **OK**.

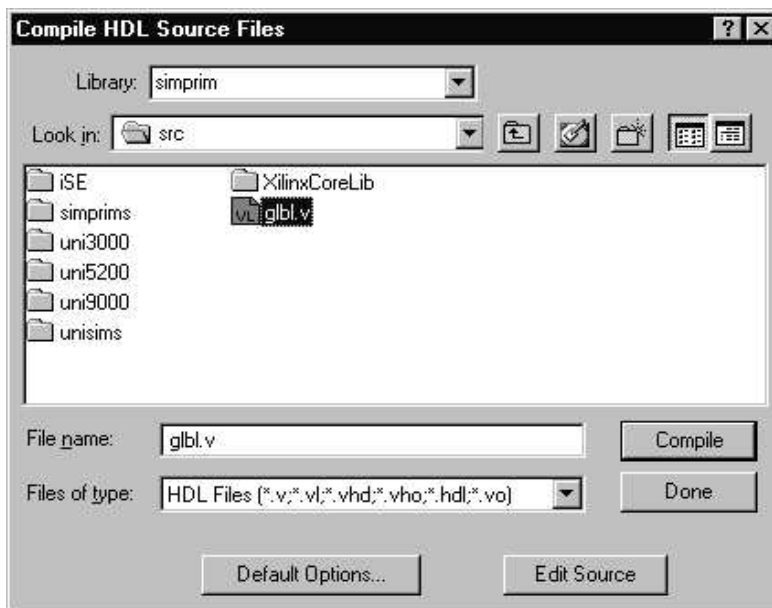


- e) Compile the simprim source files. Select the '**Compile**' button. In the 'Compile HDL Source Files' dialog box. Set the library to **simprim** using the pull down menu. Use the 'Look in' selection to locate the SIMPRIM source files. These will be found at the: **Xilinx_installation_dir/verilog/src/simprims** directory.



Select the complete list of *.v files, by selecting the first file in the list with the mouse and then selecting the last file in the list with the mouse while holding down the shift key. Select the **Compile** button.

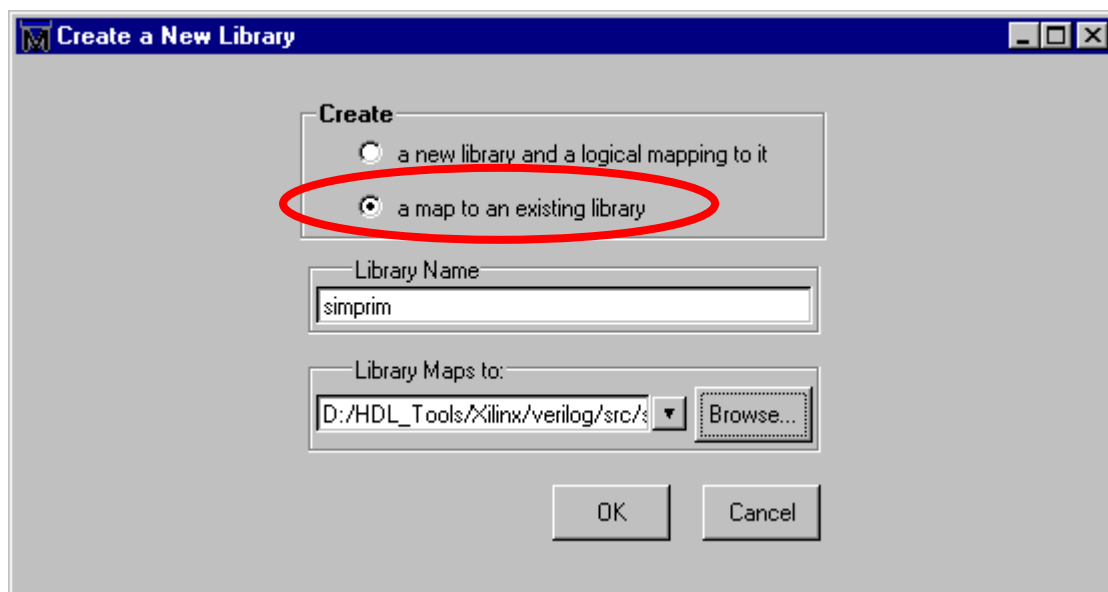
- f) Now compile the **gbl.v** file into the simprim library as well. It will be found in the: **Xilinx_installation_dir/verilog/src** directory.





3. Mapping the SIMPRIM library.

- a) Change ModelSIM directory to the ModelSIM installation directory, for example C:\Modeltech_5.5b
- b) Using Windows Explorer, change the **modelsim.ini** file properties for write permission. This file is located in the Modelsim installation directory.
- c) From the ModelSIM menu select '**Design > Create a New Library**', ensure that '**a map to an existing library**' is selected, enter **simprim** in the library name box as shown below.
- d) Use the '**Browse**' button to locate the compiled SIMPRIM library you have generated at section 2b and then select **OK**.



- e) Change the **modelsim.ini** file properties for read only.
- f) The SIMPRIM library is now ready.

4. Compilation & Simulation of the Gate-Level file.

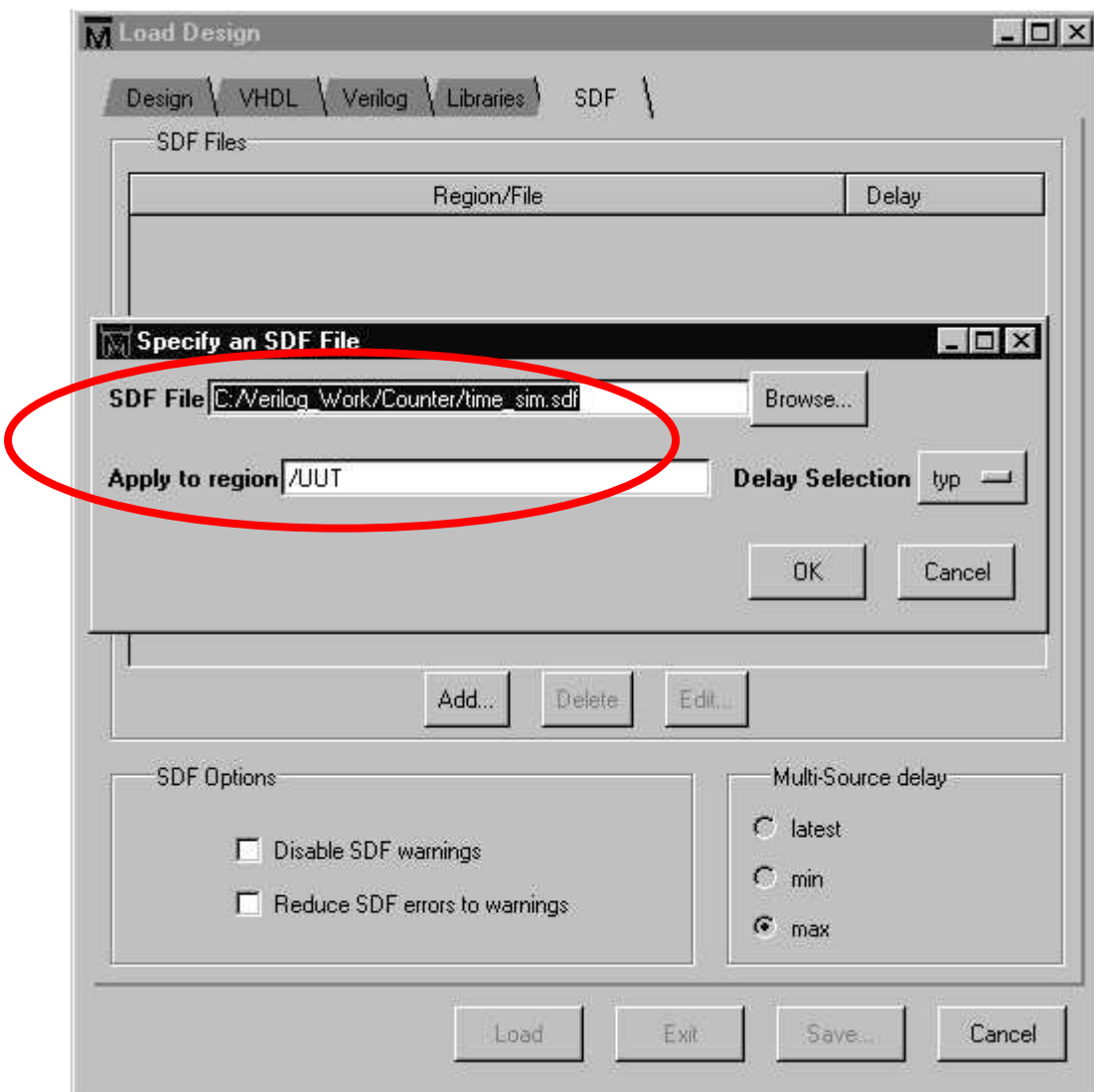
- a) Copy the **Time_sim.v** and the **Time_sim.sdf** files into your project directory.
- b) Change ModelSIM directory to your project directory.
- c) Compile the Verilog gate-level file (Time_sim.v) into your work library, using the vcom command (**vcom time_sim.v**) or from the Compile window.



- d) Select **'Design > Load Design'**.
- e) In the **'SDF'** folder select the **'Add'** option. Specify the full path to the sdf file -> Time_sim.sdf .
- e) Insert the **Instance** name of your module in the **'Apply to region'** field.

For example, in the following verilog code UUT is the Instance name:

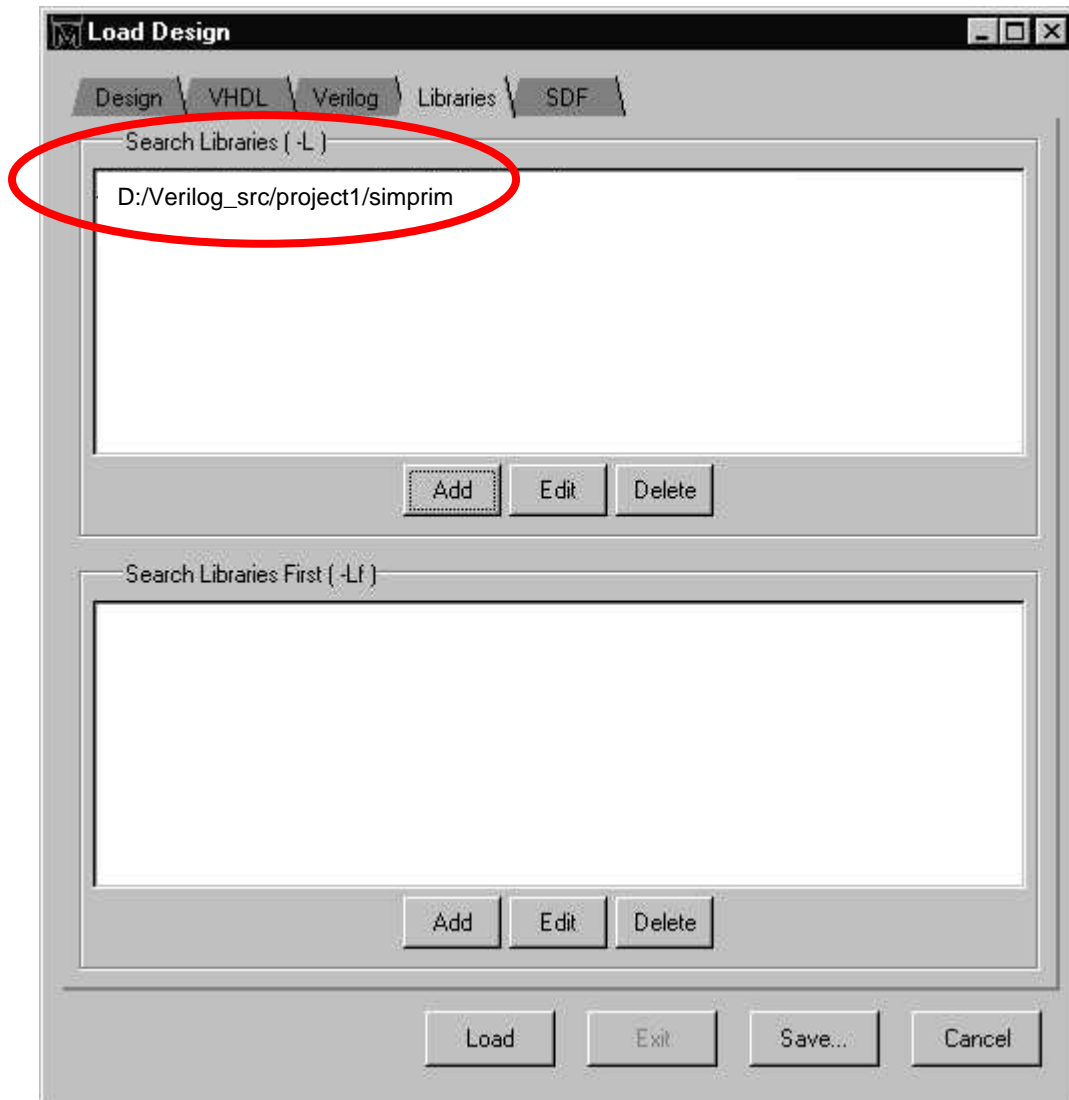
```
uart_top UUT(.clk      (clk),  
             .rst      (rst),  
             .data_in  (data_in),  
             .sin      (sin),  
             .data_out (data_out),  
             .sout     (sout)      );
```



- f) Select **OK**.



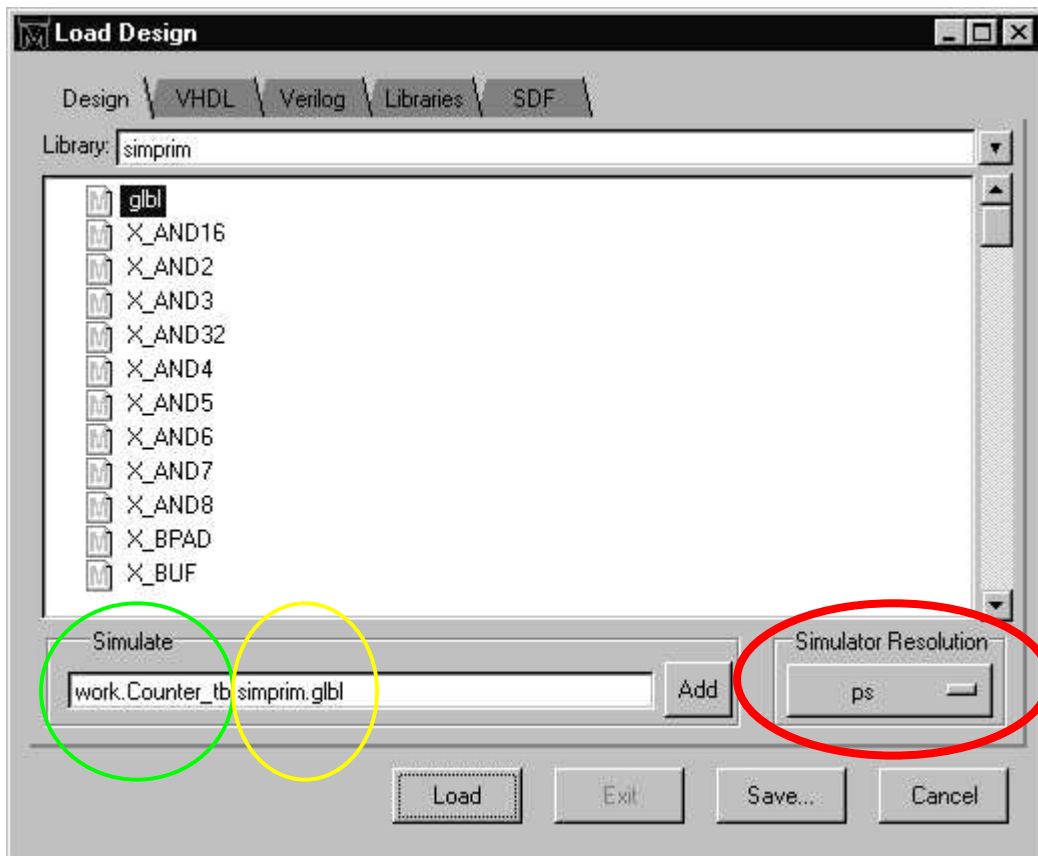
- g) In the '**Libraries**' folder add to the Search Libraries the full path to the SIMPRIM library that was generated in section 2b.





- h) In the 'Design' folder, Change the 'Simulator Resolution' to 'ps'.
- i) Set the library field to **work** and select your Test-Bench module, click the 'Add' button. In addition, you have to add the **gbl** module from the SIMPRIM library. Set the library field to **simprim** and select the gbl module, click the 'Add' button.

Your TB must be placed before the gbl module.



- j) Select the '**Load**' button to perform a gate-level timing simulation.

You may also load your design using a text command instead of using the GUI as described in sections 4 d-j by typing the following:

```
vsim -L simprim -sdfmax UUT=D:/project1/time_sim.sdf work.Counter_tb simprim.gbl
```