



SITAL Technical Notes

Adding Xilinx Chip Scope to your design with Leonardo



Assume this is your design and you want to add Chip scope:

```
library ieee;
use ieee.std_logic_1164.all;

entity chip_scope is
port(
    clk,en : in std_logic;
    d      : STD_LOGIC_VECTOR(31 downto 0);
    q      : out STD_LOGIC_VECTOR(31 downto 0)
);
end ;

architecture Sital of chip_scope is
begin
    process(clk)
    begin
        if clk'event and clk = '1' then
            if en='1' then
                q <= d;
            end if;
        end if;
    end process;
end Sital;
```

Generate the two chip scope components using Xilinx Core Gen. Instantiate these two components into your design. The problem is that these components have only input ports, thus are optimized away.

To avoid this optimization, add the NOOP attribute as seen below.

Then the design with Chip Scope would be something like:

```
library ieee;
use ieee.std_logic_1164.all;

entity chip_scope is
port(
    clk,en : in std_logic;
    d      : STD_LOGIC_VECTOR(31 downto 0);
    q      : out STD_LOGIC_VECTOR(31 downto 0)
);
end ;
```



architecture Sital of chip_scope is

```
component ila_pro
  port( CONTROL      : inout std_logic_vector(35 downto 0);
        CLK          : in     std_logic;
        DATA        : in     std_logic_vector(31 downto 0);
        TRIG0        : in     std_logic_vector(0 downto 0);
        TRIG1        : in     std_logic_vector(0 downto 0);
        TRIG2        : in     std_logic_vector(0 downto 0) );
end component;

component icon_pro
  port (CONTROL0     : inout std_logic_vector(35 downto 0));
end component;

attribute noopt : boolean;
attribute noopt of icon_pro : component is true;
attribute noopt of ila_pro  : component is true;

signal CONTROL0      : std_logic_vector(35 downto 0);
signal TRIG0         : std_logic_vector(0 downto 0);

begin
  process(clk) begin
    if clk'event and clk = '1' then
      if en='1' then
        q <= d;
      end if;
    end if;
  end process;

  i_icon_pro : icon_pro
  port map
  (
    CONTROL0 => CONTROL0
  );
  TRIG0(0) <= en;

  i_ila_pro : ila_pro
  port map
  (
    CONTROL => CONTROL0,
    CLK     => CLK,
    DATA   => D,
    TRIG0   => TRIG0,
    TRIG1   => TRIG0,
    TRIG2   => TRIG0
  );
end Sital;
```

You will need the ila_pro.EDN and icon_pro.EDN files for these two components to complete the place and route.



This is the schematic output showing the two chip scope components connected.

