



SITAL Technical Notes

Setting Internal Clocks and Clock Buffers



- 1) How do I set an internal clock buffer for internal VHDL signal or Verilog reg?
- 2) How to avoid auto insertion buffer on the clock signal?
- 3) How do I define this clock and its clock_cycle in Leonardo Spectrum?

1) In order to set an internal clock buffer in Altera/Xilinx devices, please use the buffer_sig attribute:

VHDL Example:

```
architecture behave of counter is
  signal internal_clk : std_logic;

  attribute buffer_sig : string ;
  attribute buffer_sig of internal_clk : signal is "global"; --for altera
  attribute buffer_sig of internal_clk : signal is "bufg"; --for xilinx

begin...
```

Verilog Example:

```
reg txclk;

For Xilinx:
//exemplar attribute txclk buffer_sig bufgp

For Altera:
//exemplar attribute txclk buffer_sig global
```

2) In order to avoid auto insertion clock buffer for a clock signal in Xilinx devices, (relevant when there are more clock signals in the design than clock buffers in the device) please use the “ibuf” value in the buffer_sig attribute:

VHDL Example:

```
ENTITY nobufg IS
  PORT (
    c1, r1 : std_logic;
    c2, r2 : std_logic;
    i1 : STD_LOGIC;
    i2 : std_logic;
    o1 : out std_logic;
    o2 : out std_logic
  );
  attribute buffer_sig : string;
  attribute buffer_sig of c2 : signal is "ibuf";
END ;

ARCHITECTURE sital OF nobufg IS
BEGIN

  o1 <= '0' when R1='1' ELSE i1 when rising_edge(C1);
  o2 <= '0' when R2='1' ELSE i2 when rising_edge(C2);

END sital ;
```



3) In order to define a signal as an internal clock in Leonardo Spectrum and set its clock_cycle, you have to use the **set_clock** command.

Type the following text in Leonardo command line (Leonardo level3) or include this text in a script file (all levels) after loading the design before optimizing:

```
set_clock -net -clock_cycle 20 -name internal_clock_name
```

Where 20 is 20 ns clock cycle

internal_clock_name is the internal clock signal name.

Declaring internal Clock from the VHDL or the Verilog file using attribute is impossible.