



SITAL Technical Notes

Assign Pin Numbers to Ports



How do I set pin numbers to Entity/Module ports from the VHDL/Verilog code?

Pin locations are specified in the VHDL file using the **PIN_NUMBER** and **ARRAY_PIN_NUMBER** attributes. Use the **pin_number** for individual signals and **array_pin_number** for buses.

In Verilog, only pin location for individual ports is available from the Verilog file.

VHDL Example:

```

library IEEE;
use IEEE.std_logic_1164.all;

ENTITY example IS
  Port(
    Clk16           : in std_logic;
    ResetN         : in std_logic;
    DPRAM_R_RWn    : buffer std_logic;
    DPRAM_R_OEn    : out std_logic;
    DPRAM_R_Addr   : out std_logic_vector(7 downto 0)
  );

  ----- Attribute declaration:
  attribute pin_number : string ;
  type exemplar_string_array is array (natural range <>, natural range <>) of character;
  attribute array_pin_number : exemplar_string_array ;

  ----- Pin Assignment for all devices except Altera
  Attribute pin_number of Clk16           : signal is "91";
  Attribute pin_number of ResetN         : signal is "92";
  Attribute pin_number of DPRAM_R_RWn    : signal is "213";
  Attribute pin_number of DPRAM_R_OEn    : signal is "199";

  Attribute array_pin_number of DPRAM_R_Addr : signal is
    ("100", "99 ", "8 ", "107", "193", "109", "191", "11 ");

  ----- Pin Assignment for Altera Devices only
  Attribute pin_number of Clk16           : signal is "example@91";
  Attribute pin_number of ResetN         : signal is "example@92";
  Attribute pin_number of DPRAM_R_RWn    : signal is "example@213";
  Attribute pin_number of DPRAM_R_OEn    : signal is "example@199";

  Attribute array_pin_number of DPRAM_R_Addr : signal is
    ("example@100", "example@99 ", "example@8 ", "example@107",
    "example@193", "example@109", "example@191", "example@11 ");

End;
```

Important:

- 1) When using Altera devices, the value of the attribute is "chip_name@pin_no".
- 2) When assigning pin numbers for a bus, all the strings in the bracket should be in the same length ("5 ", "109"). As you can see, in the first string there are extra 2 spaces at the end to create a 3 characters string.



In Verilog, Only pin location for individual ports is available from the Verilog file.

Verilog Example:

```
module example (  
    addr3,  
    addr2,  
    addr1,  
    addr0,  
  
    dout  
);  
  
    wire [3:0] addr;  
    input  addr3;  
    input  addr2;  
    input  addr1;  
    input  addr0;  
  
    output dout;  
  
    assign addr[3] = addr3;  
    assign addr[2] = addr2;  
    assign addr[1] = addr1;  
    assign addr[0] = addr0;  
  
// Pin Assignment for all devices except Altera  
    //exemplar attribute addr3 pin_number C1  
    //exemplar attribute addr2 pin_number D16  
    //exemplar attribute addr1 pin_number B15  
    //exemplar attribute addr0 pin_number C2  
  
    //exemplar attribute dout pin_number D2  
  
// Pin Assignment for Altera devices only  
    //exemplar attribute addr3 pin_number example@C1  
    //exemplar attribute addr2 pin_number example@D16  
    //exemplar attribute addr1 pin_number example@B15  
    //exemplar attribute addr0 pin_number example@C2  
  
    //exemplar attribute dout pin_number example@D2  
  
endmodule
```