



SITAL Technical Notes

Monitoring Internal Signals from a VHDL or Verilog Testbench



The *init_signal_spy()* utility mirrors the value of a VHDL signal or Verilog register/wire (called the *spy_object*) onto an existing VHDL signal or Verilog register (called the *dest_object*). This allows you to reference signals, registers, or wires at any level of hierarchy from within a VHDL architecture (e.g., a testbench) or a Verilog Module.

This system task works only in ModelSim versions 5.5 and newer.

VHDL Syntax: `init_signal_spy(spy_object, dest_object, verbose);`

Verilog Syntax: `Initial $init_signal_spy(spy_object, dest_object, verbose);`

Name	Type	Description
spy_object	string	Required. A full hierarchical path (or relative path with reference to the calling block) to a VHDL signal or Verilog register/wire. Use the path separator to which your simulation is set (i.e., "/" or "."). A full hierarchical path must begin with a "/" or ".". The path must be contained within double quotes.
dest_object	string	Required. A full hierarchical path (or relative path with reference to the calling block) to an existing VHDL signal or Verilog register. Use the path separator to which your simulation is set (i.e., "/" or "."). A full hierarchical path must begin with a "/" or ".". The path must be contained within double quotes.
verbose	Integer	Optional. Possible values are 0 or 1. Specifies whether you want a message reported in the Transcript stating that the <i>spy_object</i> 's value is mirrored onto the <i>dest_object</i> . Default is 0, no message.

Limitations

- When mirroring the value of a Verilog register/wire onto a VHDL signal, the VHDL signal must be of type bit, bit_vector, std_logic, or std_logic_vector.
- Mirroring slices or single bits of a vector is not supported. If you do reference a slice or bit of a vector, the function will assume that you are referencing the entire vector.



VHDL Example:

```
library modelsim_lib;
use modelsim_lib.util.all;

entity top_tb is
end;

architecture behave of top_tb is
    signal cnt_spy : integer;
begin

    :
    :

    spy_process :process
    begin

        init_signal_spy("/top_tb/uut/cnt", "/cnt_spy", 1);
        wait;

    end process;

    :
    :

end;
```

In this example, the value of "/top/uut/cnt" will be mirrored onto "/cnt_spy".

You can also [download](#) a full VHDL example from Sital Technology site (support folder) in order to simulate the Signal_Spy utility.



Verilog Example:

```
module top ();  
  
reg[4:0] cnt;  
initial cnt=0;  
  
always #37 cnt <= cnt+1;  
  
endmodule
```

```
module top_tb ();  
  
top uut();  
  
reg[4:0] cnt_spy;  
  
initial $init_signal_spy("/top_tb/uut/cnt", "/cnt_spy");  
  
endmodule
```

In this example, the value of "/top_tb/uut/cnt" will be mirrored onto "/cnt_spy".

You can also [download](#) this Verilog example from Sital Technology site (support folder) in order to simulate the Signal_Spy utility.